IN THE SPECIFICATION

The following is a clean version of an amended paragraph starting on page 20 line 27 and ending on page 21 line 14. Attachment A provides a marked up version of the paragraph showing the amendment.

The register file **216** includes a decoder, as is shown in **FIGURE 6**, for each of the sixteen read and write ports. The register file **216** includes a memory array **940** that is partially shown in the insert **910** illustrated in **FIGURE 8B** and includes a plurality of word lines **944** and bit lines **946**. The word lines **944** and bit lines **946** are simply a set of wires that connect transistors (not shown) within the memory array **940**. The word lines **944** select registers so that a particular word line selects a register of the register file **216**. The bit lines **946** are a second set of wires that connect the transistors in the memory array **940**. Typically, the word lines **944** and bit lines **946** are laid out at right angles. In the illustrative embodiment, the word lines **944** and the bit lines **946** are constructed of metal laid out in different planes such as a metal 2 layer for the word lines **944** and a metal 3 layer for the bit lines **946**. In other embodiments, bit lines and word lines may be constructed of other materials, such as polysilicon, or can reside at different levels than are described in the illustrative embodiment, that are known in the art of semiconductor manufacture. In the illustrative example, the word lines **944** are separated by a distance of about 1μm and the bit lines **946** are separated by approximately 1μm. Other circuit dimensions may be constructed for various processes. The illustrative example shows one bit line per port, other embodiments may use multiple bit lines per port.

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